In the Claims:

1. (*Previously Presented*) VLIW processor comprising:

    a plurality of functional units;

a distributed register file accessible by the functional units;

    and a partially connected communication network for coupling the functional units and selected parts of the distributed register file; characterized in that the VLIW processor further comprises communication means for coupling the functional units and the distributed register file.

2. (*Previously Presented*) A VLIW processor according to Claim 1 wherein:

    the communication means comprise a multiplexer and a bus, the multiplexer being arranged for coupling the functional units and the bus, the bus being arranged for coupling the multiplexer and the distributed register file.

3. (*Previously Presented*) A VLIW processor according to Claim 1 wherein:

    the communication means are arranged for communication with a first latency, the partially connected communication network is arranged for communication with a second latency, the first latency exceeding the second latency.

4. (*Previously Presented*) A VLIW processor according to Claim 2 wherein: the bus comprises at least one pipeline register.

5. (*Previously Presented*) A VLIW processor according to Claim 2 wherein:

    the multiplexer comprises at least one register.

6. (*Currently Amended*) A VLIW processor according to Claim 1, comprising a first plurality of functional units and a second plurality of functional units;

    a first pass unit associated with one of the functional units of the first plurality for passing data from one of the distributed register files associated with the first plurality of

functional units to one of the distributed register files associated with the second plurality of functional units;

and a second pass unit associated with one of the functional units of the second plurality for passing data from one of the distributed register files associated with the second plurality of functional units to one of the distributed register files associated with the first plurality of functional units.[[;]]

7. (*Previously Presented*) A VLIW processor according to Claim 6 wherein:

the pass units are part of the respectively associated functional units.

8. (*Previously Presented*) A VLIW processor according to Claim 1 wherein:

the communication means couple the functional units and all parts of the distributed register file.

9. (*Cancelled*)